TIMING SUBSYSTEM DEVELOPMENT - NETWORK SYNCHRONIZATION EXPERIMENTS

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ABSTRACT

In the prodominantly digital Defense Communication System (DCS), a requirement exists to coordinate clocks at geographically distinct nodes to handle switched digital traffic and provide a general timing capability. The characteristics of the nodal clocks, link equipment delay/phase relationships, transmission medium, and synchronization technique all affect system performance and must be considered when attempting network-wide clock alignment. This paper describes a program in which several experimental timing subsystem prototypes were designed, fabricated, and field tested using a small network of troposcatter and microwave digital communication links. This equipment was responsible for modem/radio interfacing, time interval measurement, clock adjustment and distribution, synchronization technique, and node-to-node information exchange. Presented are discussions of the design approach, measurement plan, and performance assessment methods. Recommendations are made based on the findings of the test program and an evaluation of the design of both the hardware and software elements of the timing subsystem prototypes.

INTRODUCTION

The DCS network involves a large number of links and nodes with various categories of transmission media, including troposcatter (TROPO), line-of-sight microwave (LOS), satellite, and cable. The variety of transmission equipment that is available now, or planned as part of an all-digital network, makes a complete and comprehensive evaluation of system performance difficult; therefore, an emphasis in the experimental work reported on here has been toward synchronization performance in a three

node network at RADC, Rome, NY.

As speed, size, and complexity of military communications systems increases, characteristics of the frequency sources that clock digital information play a more dominant role in determining the overall effectiveness of the system. If the desired goal is to provide a synchronous non-interrupted digital network, then even a modest amount of clock disciplining would greatly ease the problem. Since each separate node would have a frequency/time source, it has traditionally been considered paramount that each be of highest quality to minimize clock-to-clock relative drift and maximize the time between buffer resets (which interrupts digital traffic). In practice, the continuous traffic goal is unattainable when operating in an independent clock mode; buffer resets would still be required. This places the burden on the clocks themselves and the system designer is forced to specify highly accurate, highly stable, and very costly standards. For planned networks with literally hundreds of nodes, the cost is substantial.

A directed-control disciplined network rests the network frequency (phase) reference with one or at most, a few of the best sources while subordinate clocks are manipulated to follow the characteristics of the selected references. These manipulated clocks need only be lesser-quality (i.e., quartz) standards since their individual frequency trends are not mapped throughout the network.

An active clock control situation must rely on a timing/synchronization technique to carry out the timing function and insure a stable, reliable system. The focus of the Timing Subsystem Development program was to design, build, and test equipment to achieve this end using an existing Air Force network for evaluation [1]. Although several techniques have been proposed and studied [2] - [6], as yet an actual field implementation had not been attempted.

This paper begins with a brief review of time transfer techniques and objectives. The microprocessor-based link termination and processing equipment is described revealing the hardware and software components of the system. Following an overview of the RADC network configuration, a summary stemming from laboratory experience and field experiment findings forms the base on which relevant observations, conclusions, and recommendations are presented.

BACKGROUND

The primary mechanism for clock comparison is the transfer of digital data over links terminated by node processing equipment. At any node, incoming data is clocked into a buffer by signals derived from the receiver-demodulator bit tracking loop. This clock signal exhibits fluctuations and drift behavior as a result of transmit clock variations, medium variability, and tracking loop dynamics. In a synchronous network, the received data is later clocked out of the buffer by the node clock and multiplexed or switched with other data from other terminated links for retransmission; the objective being to coordinate the collection of node clocks so that buffers do not overflow or deplete. For normal communication, relative synchronization of the nodes is sufficient and the node clocks need not be phased identically as long as their mutual average frequency offsets are zero. In addition, a timekeeping function would involve the desire to meet the above objective with zero phase offset between node clocks. Combined with removal of ambiguity, phase-aligned clocks serve as the basis for a time-of-day distribution system. A scheme of this type has obvious advantages when the network is referencing universal time such as UTC. Time is marked at each end of the link in terms of a periodic Time Reference Pulse (TRP) which is synchronous with the high rate data clock. If ambiguity issues are ignored in this discussion, it can be simply stated that the time transfer objective is to align TRP transmissions.

The data required in the clock control loop processor will depend on synchronization technique selected (timing algorithms reside in firmware) but, in general will consist of time measurements from two nodes, A and B, of a TRP. Node B measures the elapsed time of the incoming TRP from node A relative to its own clock, resulting in the quantity t_A. Similarly, at node A the TRP from node B is measured relative to the local clock producing t_B. Defining the clock TRP emission times on a reference time scale to be t'_A and t'_B, the four parameters are:

t'_A = node A transmit TRP relative to node A reference

t_B = node B receive TRP relative to node A reference

t'_B = node B transmit TRP relative to node B reference

t_A = node A receive TRP relative to node B reference

Considering a path delay from A to B as $\mathcal{T}_{AB}$, it can be shown that for a single-ended transfer, TRP arrival time at node B relative to node A is:

$$\mu_{AB} = t'_A - t_A + \mathcal{T}_{AB}$$

and TRIP arrival time at node A relative to node B is:

$$\mu_{BA} = t'_B - t_B + \mathcal{T}_{BA}$$

For double-ended exchanges the clock difference is:

$$\mu = 1/2\ (t'_A - t_A - t'_B + t_B)$$

Path delay can be computed as:

$$PD = 1/2\ [(t_A + t_B) - (t'_A + t'_B)] \text{ assuming } \mathcal{T}_{AB} = \mathcal{T}_{BA}$$

All parameters are to be interpreted as elapsed time measurements. Figure 1 illustrates these clock error and path delay calculations for single- and double-ended exchanges using TRP's derived from Time Reference Information Packets (TRIP's).

In a synchronous network, incoming data enters an elastic store at a rate determined by the receiver tracking loop output, but is clocked out of the store at a rate determined by the local node clock. Differences are accommodated as long as buffer capacity is not exceeded, and date is transmitted out of the node without the need for pulse stuffing. Although not classified as synchronous, the independent clock approach follows this methodology but, buffer resets are inevitable when input/output rates differ without correction.

With the current timing subsystem design, implementation of the various timing techniques differs only in the way references are selected or combined. Considering the once-per-second update rate, processor execution speed for each technique is not significant and, in each case, the result is a clock phase or frequency shift command to alter the node reference 1-pps signal. Similarly, the phase control indirectly affects buffer clocks causing the rate of fill or depletion to change. With independent clock operation, the phase shift control is zeroed.

TIMING SUBSYSTEM PROTOTYPE

The basic function of the Timing Subsystem (TS) is to combine locally-made timing measurements with other timing information transmitted from connected nodes in order to compute local clock error relative to a master reference. The nature of this reference is determined by the synchronization technique in effect. Then, based on the computed clock error, the TS corrects its local node clock and transmits local timing information to other nodes. A photograph of the three TS prototypes and development station is shown in Figure 2.

The TS is configured of several modules, each with a particular function. Many of these modules are under the control of a Central Processing Unit (CPU) which determines the order of events, performs arithmetic tasks, and collects information for performance evaluation and general system monitoring. Each TS contains the following sections; CPU, time interval measurement unit, clock control and distribution, frequency synthesizer, multiplexers for data input and output, and other interface circuitry. A block diagram is shown in Figure 3.

NODE CONTROL COMPUTER AND SOFTWARE

The TS is microprocessor-based equipment designed around the Motorola 6800 8-bit MPU and support devices. Floating point arithmetic functions are handled by a separate arithmetic processor chip. Figures 4 and 5 depict the bus-oriented control processor and I/O structure. During design, and effort was made to keep as much of the hardware as possible under computer control. This maximized the flexibility of the system by shifting much of the application-specific configurations to the software. Similar to the hardware structure, nodal software is divided along functional boundaries. Many routines are entered through external interrupt and relative asynchronism between rountine execution is controlled by a special interrupt dispatcher that maintains a prioritized queue of scheduled processes [7]. The interrupt dispatcher determines the order of events and insures that no process will begin unless certain conditions have been satisfied. Figure 6 is a functional block diagram illustrating the various program modules incorporated in the TS software.

The user interface to the timing subsystem consists of a software monitor and debugger that allows the operator to set

up experiments by defining memory locations and initiating a run. The monitor responds to simple commands and is always available to the user (even during an experiment). Several timing functions and system configurations may be invoked by manipulating the set-up parameters through the operator keyboard. In this light, the TS can be considered a programmable device cable of clock error measurement, control, and distribution.

Software development was made less cumbersome through the use of a microcomputer development system. It can also be used as an intelligent terminal to provide general communication and data-logging functions. Experiment set-ups can be stored on disk and down-loaded to the TS.

LINK TERMINATION

Special-purpose link termination processors support the clock data communications through service channel multiplexers. These can be wired to accommodate many of the standard military data rates. In particular, they follow the Synchronous Data Link Control (SDLC) protocol. Information frames contain the timing and status indicators and are of programmable length (typically 536 bits). A flag detect circuit provides a pulse to the time interval measurement unit to mark time-of-arrival at the same point for each frame. A 16-bit cyclic redundancy check feature indentifies the presence of bit errors. Due to the fact that critical timing information is contained in these frames, errored TRIP's are discarded.

TIME INTERVAL MEASUREMENT

The basic criteria required to determine clock error is derived from direct measurement of once-per-second pulses from divided-down, buffered 5 MHz frequency standard outputs. Resolution of +/- 10 ns is obtained through the use of a 100 MHz counter with multiple output registers. On each connecting link there is a transfer of timing events and control signals. This data is transferred in blocks (TRIP's) separated by frame markers that emanate from each node at a rate of once-per-second. TRIP data format is shown in Figure 7. Time-of-arrival resolution is 10 ns and the date rate is 4 KHz via the service channel for all nodes.

CLOCK CORRECTION AND PERFORMANCE ASSESSMENT

The fundamental function performed by the clock correction control loop is the generation of a set of reference frequencies, derived from a 5-MHz node reference, to avoid buffer overflow or depletion. The unperturbed standard output is called the station standard and the adjusted version of this signal is called the node reference. A phase shifting device implements the correction in response to a digital control command. The shifted output from this device then goes to a digital clock which supplies a 1-pps time reference to all equipment at the node, and in particular, to the time-of-arrival measurement device.

TS-based performance assessment consists of storing a series of 10-minute averages of computed clock error, path delay (for double-ended exchanges only), and averages of node reference clock vs. up to three external 1-pps signals. By connecting external pulses for comparison, nodal drift may be compared to any other clock or, by trace-back through additional receivers, to a LORAN-C signal, and ultimately, to U.S. National Time Standards.

NETWORK CONFIGURATION

TROPO AND LOS LINKS

A small tandem network (three nodes, two single-ended links) consisting of a troposcatter and microwave link was configured at RADC, Rome, NY. The RADC test sites included modem and radio equipment to support the links. Figure 8 indicates the geographical layout of the sites used in the field test program. The Verona and GAFB locations were connected by a LOS link through a repeat station at Stockbridge (normally left unattended). Philco-Ford LOS baseband modems operating at 3.088 MHz were used in conjunction with Philco-Ford LC-8D radios broadcasting in the 8 GHz region. A one-way medium-only delay of 138.3 μs over 25.7 miles was observed. Timing variations were typically less than 10 ns.

An important aspect of the link selection process was to evaluate the performance of a fading channel when used to support a timing function. At the time, the Youngstown-to-

Verona TROPO path (168 statue miles) was available and configured with Raytheon DAR-IV digital modems and AN/TRC-132A radios operating at 3.5 MHz over the 4.4 - 5.0 GHz band (C band), respectively. A one-way medium delay of 910.1 μs with variations of about $\pm$20 ns was verified [8].

CONNECTING THE TIMING SUBSYSTEM

At each link termination site, the TS units were connected directly to modems and radios. A MUX hierarchy was not used. TRIP flag sequences generate a reference pulse at each receiver to stop the interval counter. Combined with transmit timing information contained in the TRIP, a clock error term can be computed. For single-ended transfers, average path/equipment delay must be included to eliminate a phase offset that would otherwise be the result.

As an example of node configuration, Figure 9 shows the connections required at the Verona site as middle node in a tandem network. In an effort to improve monitorability and measurement reliability, NBS-developed Frequency Measurement Terminals (FMT's) were used to measure the same pulses that the TS's were logging. Also, from each FMT, a decoded LORAN-C 1-pps signal was connected to one of the TS auxiliary inputs for direct comparison to the nodal station standard. Thus, each TS measured and stored the LORAN-C signal relative to its adjusted clock; giving a level of redundancy. This provided a means to evaluate clock trends compared to an unadjusted ultimate reference or, any other site standard.

MEASUREMENT AND REFERENCE FACILITIES

The choice of frequency source for each TS station centered around availability. If at a given site, a frequency source was not available, the TS employed its own internal source to allow stand-alone operation. During the design phase of this program, it was anticipated that, in certain tests, the TS's would be equipped with atomic standards. Therefore, space was provided in the chassis for such units. However, two of the three TS's also contained VCXO's for stand-alone operation and to compare the performance of these devices with higher quality standards. Under this configuration, the TS oscillator was used to drive the internal synthesizer and frequency distribution system. It was observed that the characteristics of the quartz devices are quite satisfactory when operated in the slaved mode. Furthermore,

the high servo update of 1 per second is well-matched to the use of quartz sources in the subsystems.

A single telephone interface was wired using data couplers furnished by the FMT's. Nodal management, setup, and parameter transfers were accomplished by accessing each TS individually. Through this technique, control and management functions were handled by using a remote terminal and dialing telephone numbers. This is acceptable for a small network but a large network (i.e., greater than six nodes) would benefit from a node management protocol (for the purpose of network configuration) gaining TS control through TRIP data packet exchanges originating from a single controller and propagating around the network.

EXPERIMENTS

EQUIPMENT DELAY

The TS equipment can be used to measure round-trip delay in modems and radios if they can be configured in loop-back mode. Actually, for the purpose of directly measuring round-trip path and equipment delay, a loop-back through the transmission path with a single TS both as source and sink yields the cumulative delay of all link elements. Generally, a survey of individual delays of each piece of link equipment is required to properly configure an experiment. This procedure will help to identify any asymmetric signal propagation properties so they can be accommodated at set-up time. For double-ended exchanges, any difference in opposite-path delays will manifest itself as a phase offset superimposed on clock-correction terms. Directed-control schemes rely on frequency averaging so equipment delay compensations need not be included if frequency tracking is the desired result.

FIELD EXPERIMENTS

Emphasis in the experiment series was placed on observing basic network synchronization through node-to-node clock error logging. Time did not permit more extensive evaluation of such things as: phase alignment, alternate tracking loop bandwidths, multiple stage acquisition strategies, and tier-type self-organizing timing techniques. Furthermore, due to link equipment availability, only a tandem, single-ended exchange network configuration was possible.

The Seneca, NY, LORAN-C station was considered to be the ultimate network reference. This station is slaved to the Dana, IN, East coast chain master. Since experiments were concerned with frequency alignment, a calibration procedure determined the relative frequency drift between the LORAN pulse and each site standard. GAFB and Verona employed rubidium sources. Youngstown used a cesium clock. Through receivers located in each FMT (one at each site) LORAN-node relative frequency trends were measured and plotted as shown in Figure 10. Small variations are smoothed so the plots represent average trends. Data was gathered over a period of about eight days. Notice that each site standard is drifting in the same direction. Although not usually the case, it was assumed that each source was drifting at a constant rate; short-term stability tends to be better for rubidium sources than for cesium clocks. Most importantly, this frequency comparison forms the basis for evaluating node performance, since the TS's use the site standards directly as a timing source to drive station interval measurement devices and synthesizers, and all performance assessment measurements are made relative to each site standard.

Testing consisted of a series of six relatively short experiments. Run times varied between 24 and 48 hours. Each used the directed control type of synchronization, one with automatic master selection. Typically, an experiment session proceeds as follows:

- Select an ultimate, unadjusted reference through which the performance of each node can be compared.
- Determine the frequency offset of each site standard compared to the ultimate reference.
- Configure the network for a timing experiment, including node parameters and connections for evaluation equipment.
- Permit experiment to run for at least 24 hours so that acquisitional effects, and other short-term perturbations, do not significantly affect the measurement series.
- Compare resulting time interval measurements of the adjusted TS clock with those of each unadjusted site standard. These measurements can be collected through

either the FMT, TS, or both.

- Plot the frequency offset between the TS adjusted clock and the unadjusted site standard (maintain directionality).

- Add or subtract the frequency offset of the site standard compared to the ultimate reference. The result is the net frequency error. Frequency comparisons may be either node-to-node or node-to-ultimate reference.

Table 1 summarizes network performance for each of the six experiments. Experiment 4 ran with the original version of time reference distribution including the path length counter [4]. Experiment 5 used master/slave for synchronization but superimposed a much larger frequency offset on the master node to simulate a poor clock. Reading across Table 1 illustrates that each TS was able to accommodate the added offset which was set at 2.8×10^{-9}. Experiment 6 incorporated the use of a quartz VCXO in the GAFB slave node to evaluate its performance as a station standard. To the limits of available measurement capability, the quartz slave performed admirably with only slightly higher short-term fluctuations. In each case, test results show that the network had in fact, achieved frequency alignment and stable operation. For these experiments, inverse tracking loop noise bandwidths were 45 Hz and 450 Hz for LOS and TROPO links, respectively.

CONCLUDING REMARKS

Observations made during performance evaluation indicate that steady-state frequency tracking between geographically distant nodes was achieved. By referencing an unadjusted clock, the relative drift of each of the nodal clocks was compared. Experiments support conclusions from [8] that timing information can be successfully transferred over both LOS and TROPO channels. For this series of experiments, time interval measurements were triggered directly from received packets. When a multiplexer hierarchy exists, alternate reference pulse extraction schemes through MUX or radio framing patterns, are within the capabilities of the existing TS design.

It should be evident that the timing subsystem prototypes are capable of implementing and evaluating many different arrangements in network architecture and synchronization technique. Recently, a set of desirable attributes for the DCS switched digital network was proposed [9], [10] as enhancements to a basic directed control approach offering features considered important in a military environment. The TS prototypes can easily be programmed to employ these attributes.

The TS hardware is arranged around a general-purpose microprocessor architecture and the I/O devices can deliver a wide range of data rates and MUXing schemes. The equipment was found to be quite reliable with a computed MTBF of 1400 hours [11] substantiated by zero failures in the field after periodic use over a span of about six months. Generally, microprocessor-based designs are particularly suitable for use in timing and synch applications.

Considering the somewhat restricted testing schedule for this program, it is strongly encouraged that further experimentation be undertaken. To investigate some of the more pressing issues, additional tests should include the evaluation of: acquisition and tracking strategies, single-ended vs. double-ended exchanges, precise time techniques, and the level of network automation. For example, a network management protocol could be easily implemented through existing overhead space in the TRIP's. This would centralize control for start-up and monitoring purposes but would not jeopardize the function of distributed references and self-organization.

In military applications requiring clock control, survivability, reliability, maintainability, and monitorability take on much more emphasis: the timing subsystems reported on here already possess these features to some degree. A more difficult problem is that of selecting a general approach for a timing technique, and more precisely, phase referencing or frequency alignment. A directed control system (master/slave) is most often recommended as the best compromise, especially if one of the more urgent requirements is to eliminate digital traffic interruptions inherent in independent clock networks. Mutual synch systems are not considered good candidates for DCS applications [1], [5], [6]. Several tactical programs (JTIDS, SEEK-TALK) specify the use of high quality frequency standards [12] maintaining that buffer resets will be infrequent when clocks

run independently. Even a minimal timing function would improve link availability and overall reliability while at the same time make possible replacement of some expensive standards with quartz sources.

The Timing Subsystem Development program has demonstrated that communication link termination, clock control and correction, network synchronization and performance assessment capabilities can be implemented using a single microprocessor-controlled device. Furthermore, there is ample evidence that the current design can support the interfacing and processing requirements for advanced testing well into the foreseeable future.

ACKNOWLEDGMENTS

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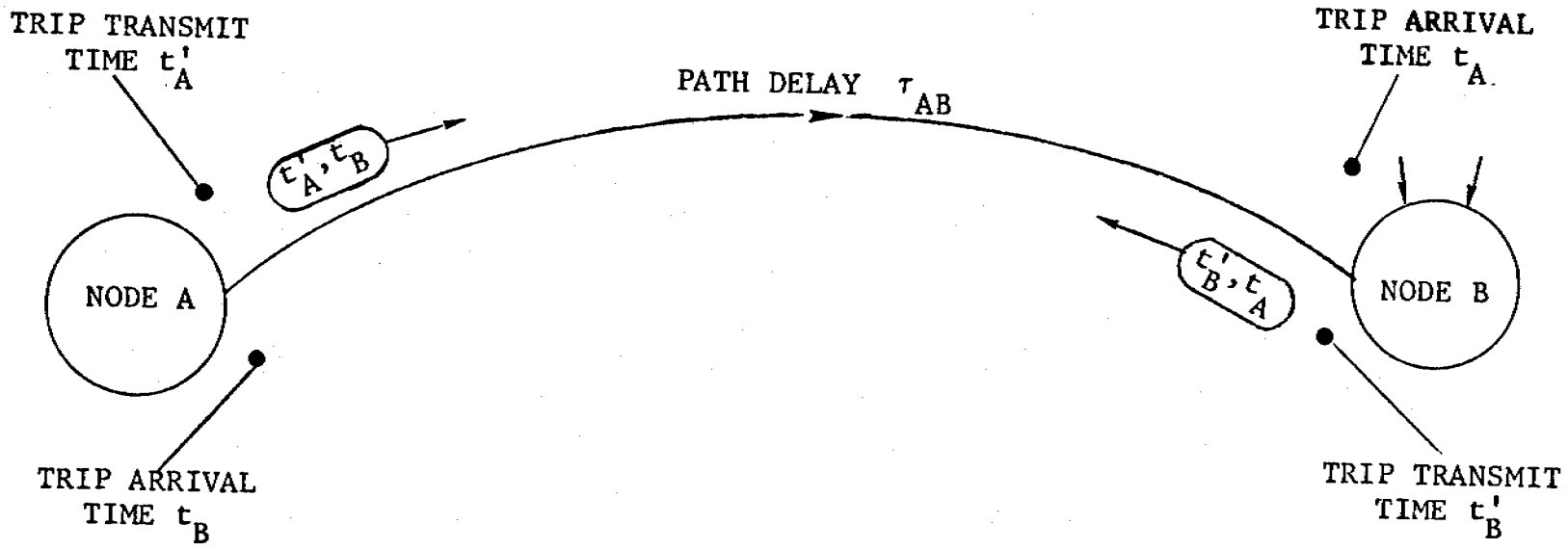


TRIP ARRIVAL TIME AT B (RELATIVE TO A) $= t'_A - t_A + \tau_{AB}$

TRIP ARRIVAL TIME AT A (RELATIVE TO B) $= t'_B - t_B + \tau_{BA}$

} SINGLE-ENDED COMPUTATION

CLOCK ERROR (EQUAL DELAYS) $u = \frac{1}{2}(t'_A - t_A - t'_B + t_B)$

$=$ CLOCK A - CLOCK B (START-TO-STOP TIME)

} DOUBLE-ENDED COMPUTATION

PATH DELAY $\tau_{AB} = \frac{1}{2}\left[(t_A + t_B) - (t'_A + t'_B)\right]$ ASSUMING $\tau_{AB} = \tau_{BA}$

Figure 1 Clock Error and Path Delay Calculations for Single- and Double-Ended Exchanges

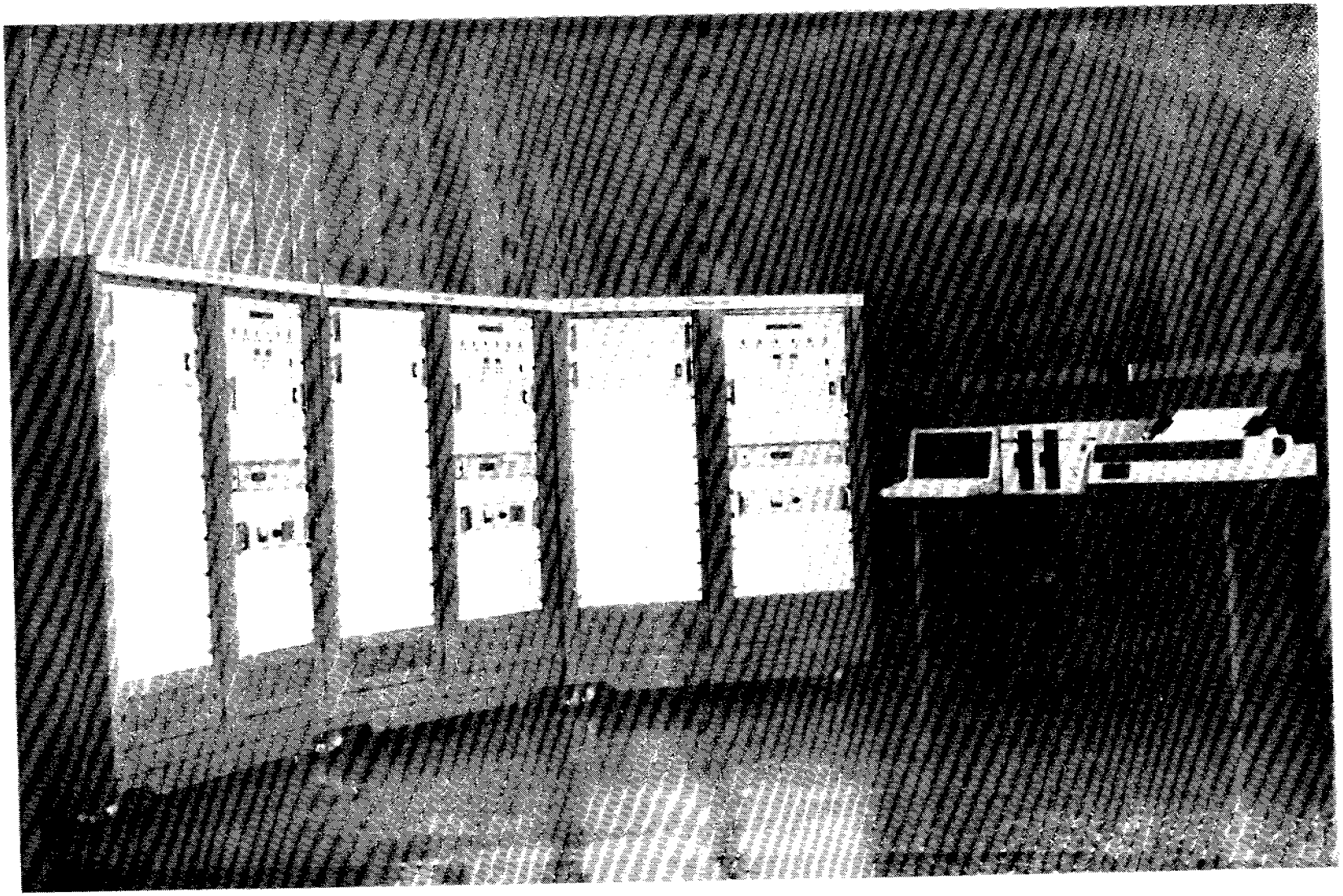


Figure 2 Timing Subsystems (3) with Microcomputer Development Station

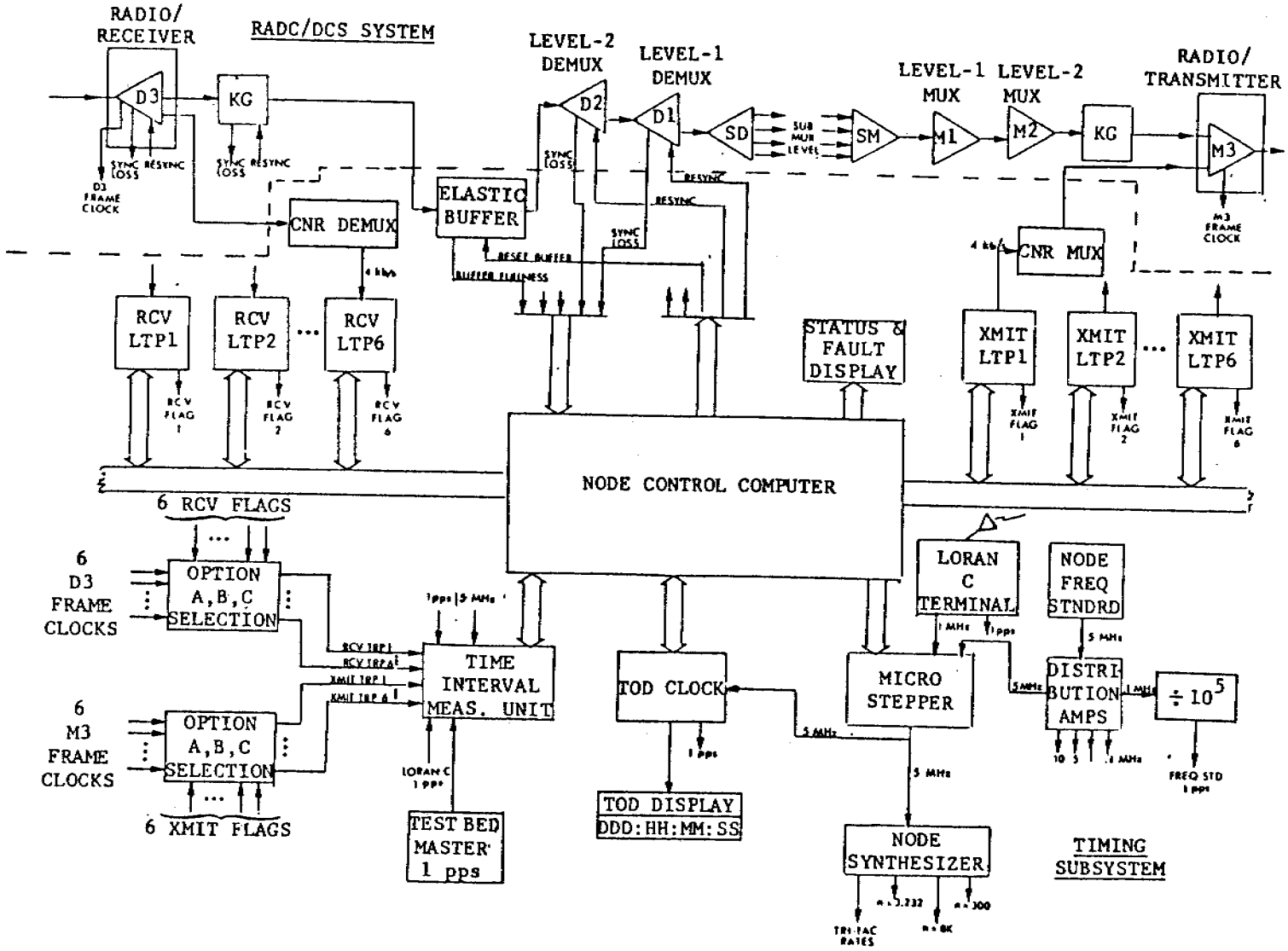


Figure 3 Block Diagram of Timing Subsystem Showing Interfaces with Link Multiplexers

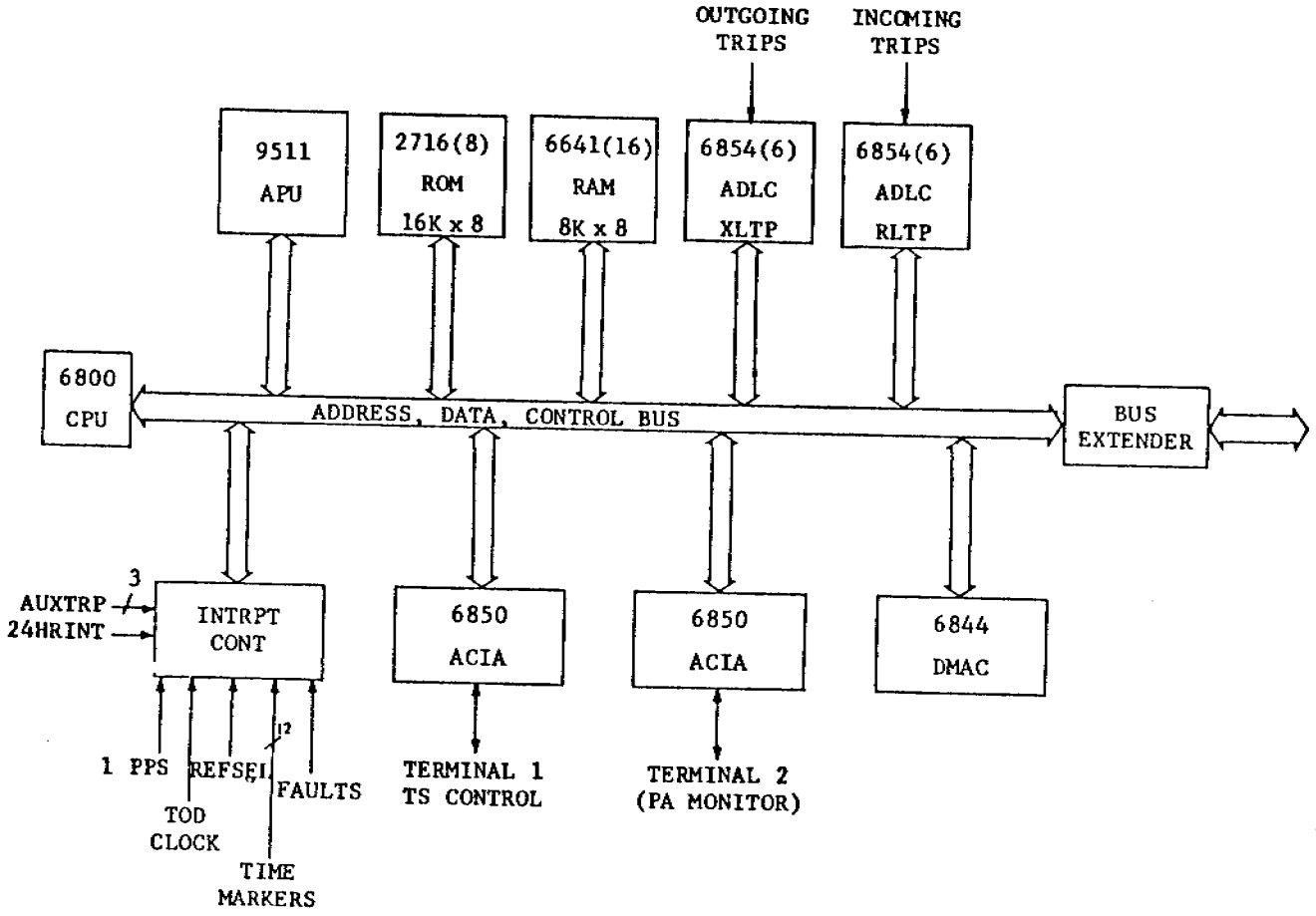


Figure 4 Node Control Processor

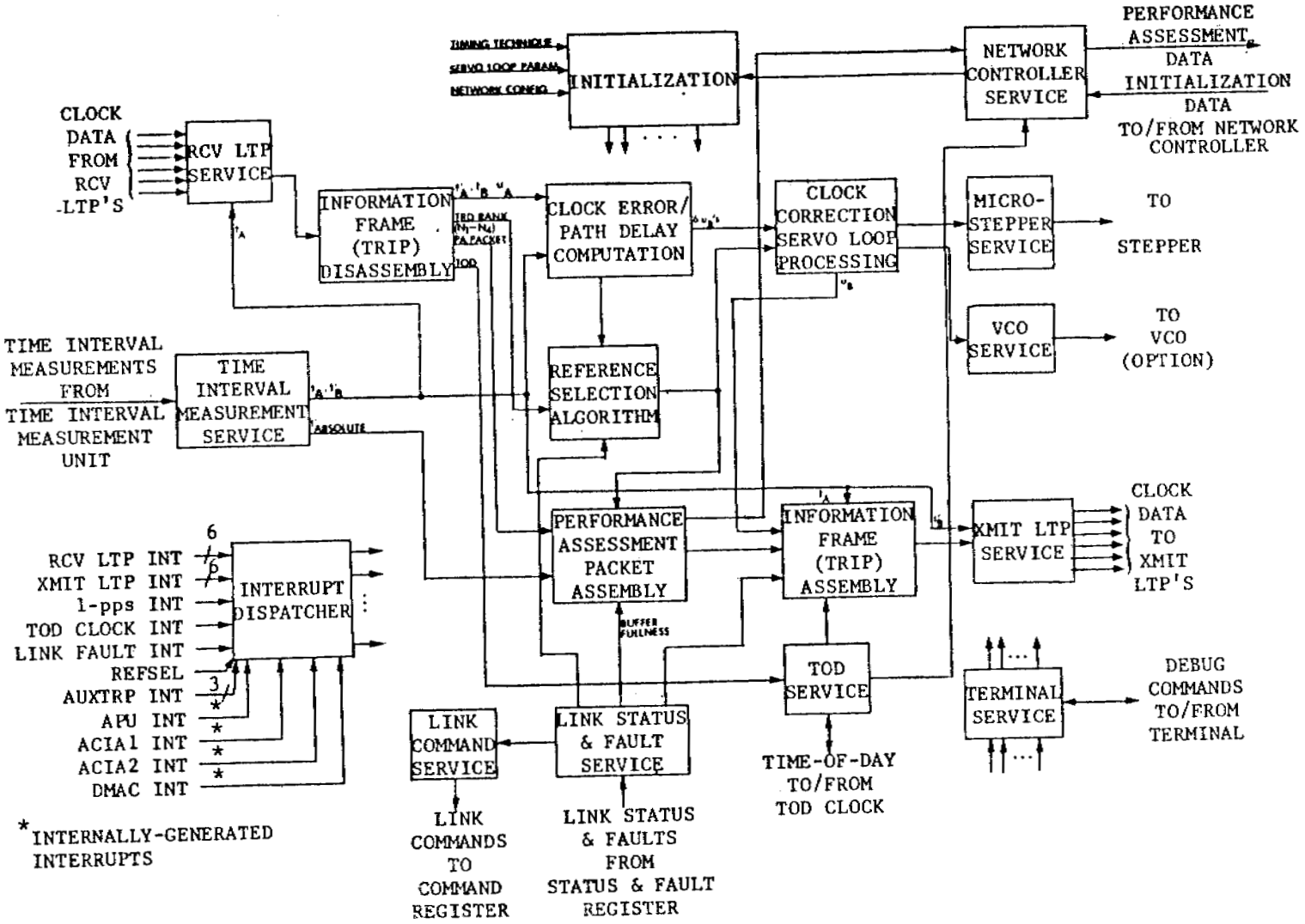


Figure 5 Node Control Computer Functional Block Diagram

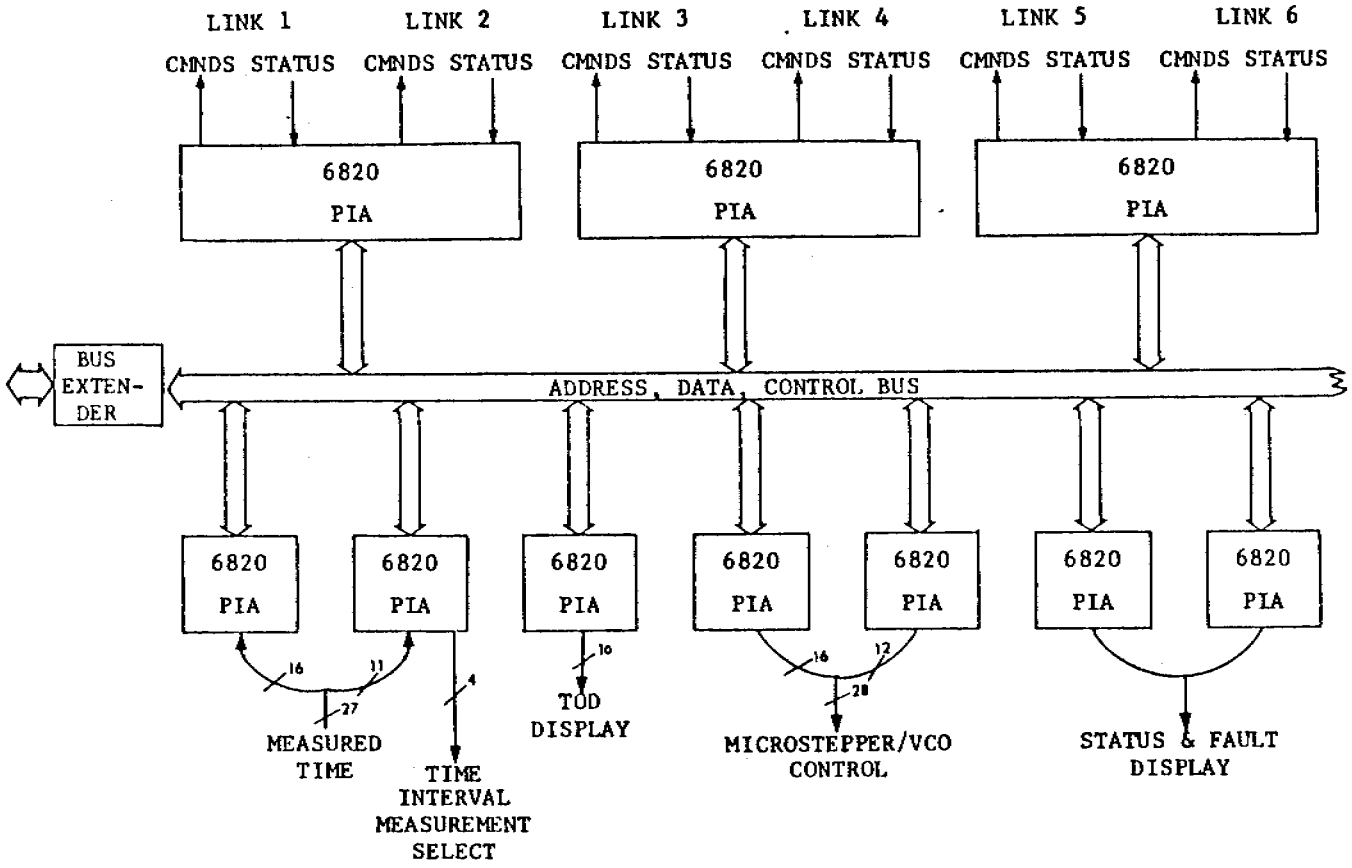


Figure 6 Parallel I/O

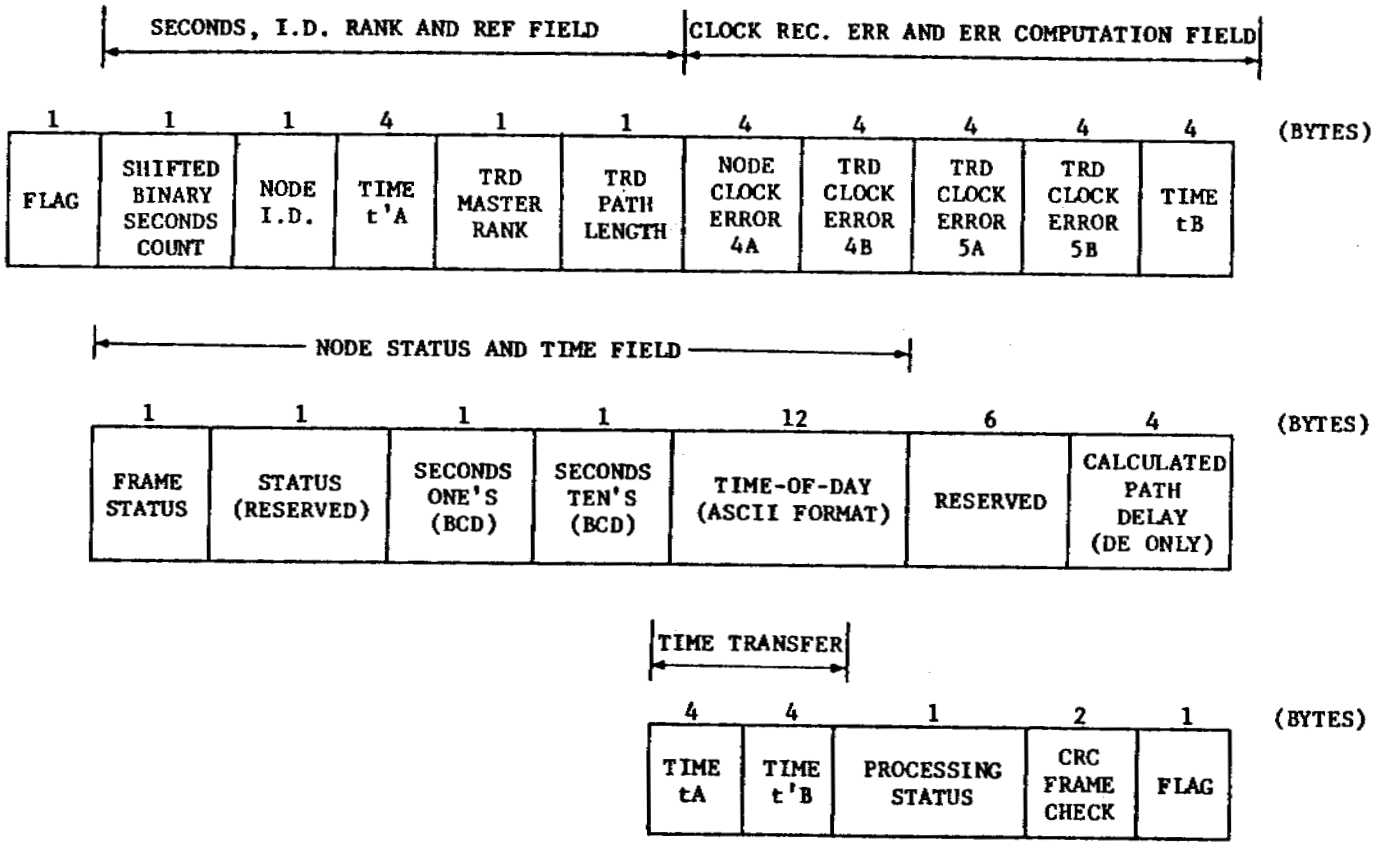


Figure 7 Clock Data TRIP Format

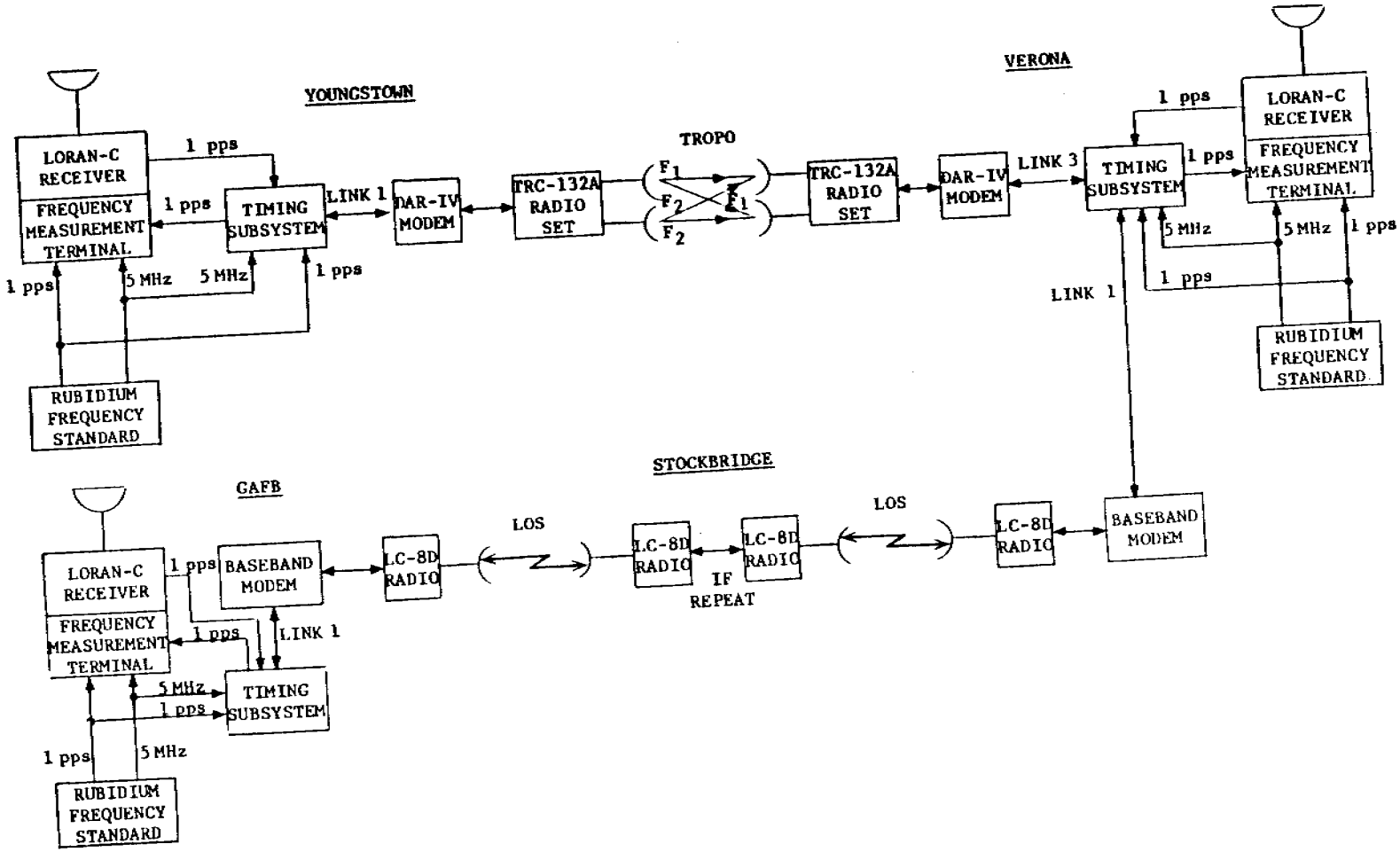
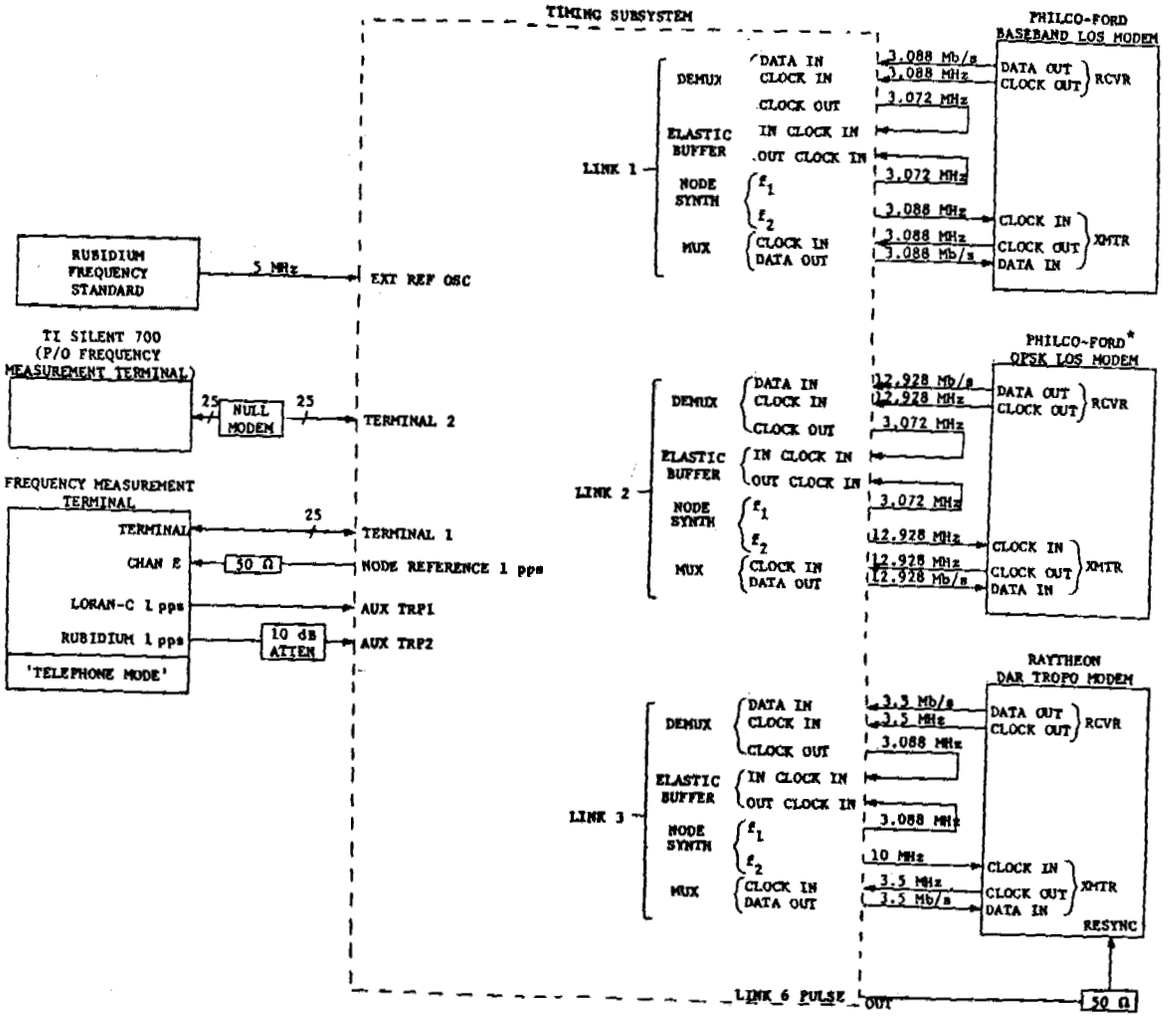


Figure 8 Three-Node Tandem Network with LOS and TROPO Links



* This link not used.

Figure 9 Node Configuration (Verona)

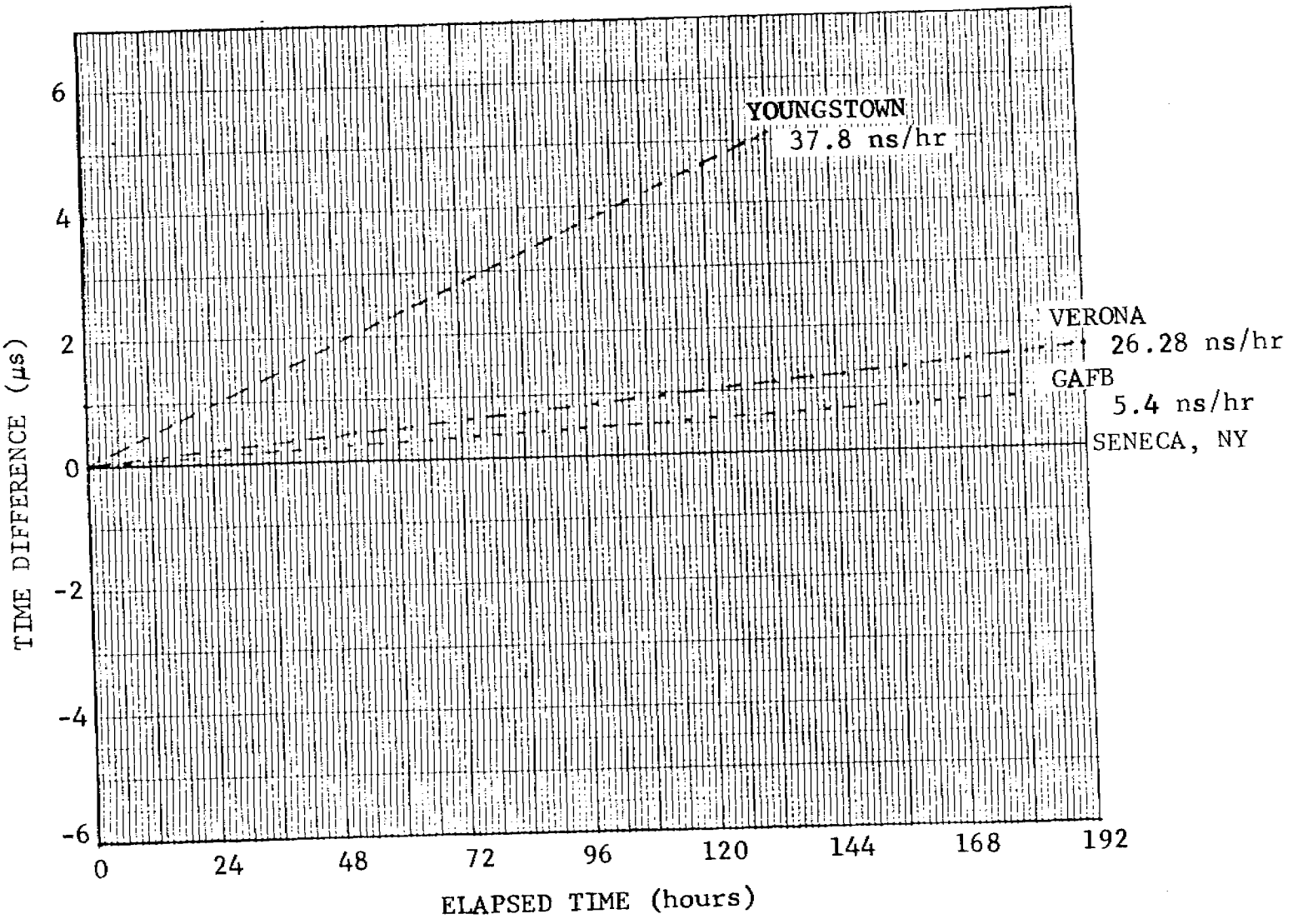


Figure 10 Seneca, NY, LORAN-C Station Frequency vs. Unadjusted Node Frequency Standards

TABLE 1

SUMMARY OF NETWORK SYNCHRONIZATION PERFORMANCE*

		FREQUENCY OFFSET AS COMPARED TO LORAN-C SENECA, NY		
EXPERIMENT	TYPE	YOUNGSTOWN	VERONA	GAFB
Site Standard	Free Running Rubidium Standard	1.05×10^{-11}	7.3×10^{-12}	1.5×10^{-12}
1	2N-M/S	1.05×10^{-11} (Master)	1.03×10^{-11}	--
2	2N-M/S	--	2.3×10^{-12} (Master)	2.3×10^{-12}
3	3N-T-M/S	1.05×10^{-11} (Master)	1.05×10^{-11}	1.05×10^{-11}
4	3N-T-TRD	1.05×10^{-11} (Master)	1.05×10^{-11}	1.05×10^{-11}
5	3N-T-M/S Master-Lrg. Freq. Offset	2.8099×10^{-9} (Master)	2.8×10^{-9}	2.8×10^{-9}
6	3N-T-M/S Slave VCO	2.8099×10^{-9} (Master)	2.8×10^{-9}	2.81×10^{-9}

*Read across to determine node-to-node frequency offset.

QUESTIONS AND ANSWERS

None for Paper #20